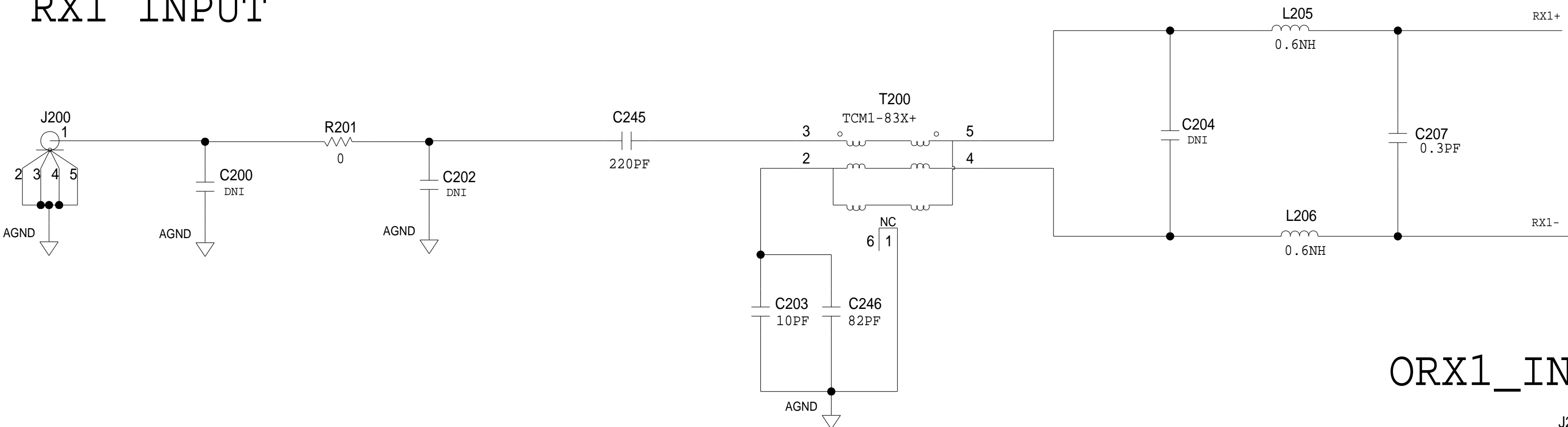


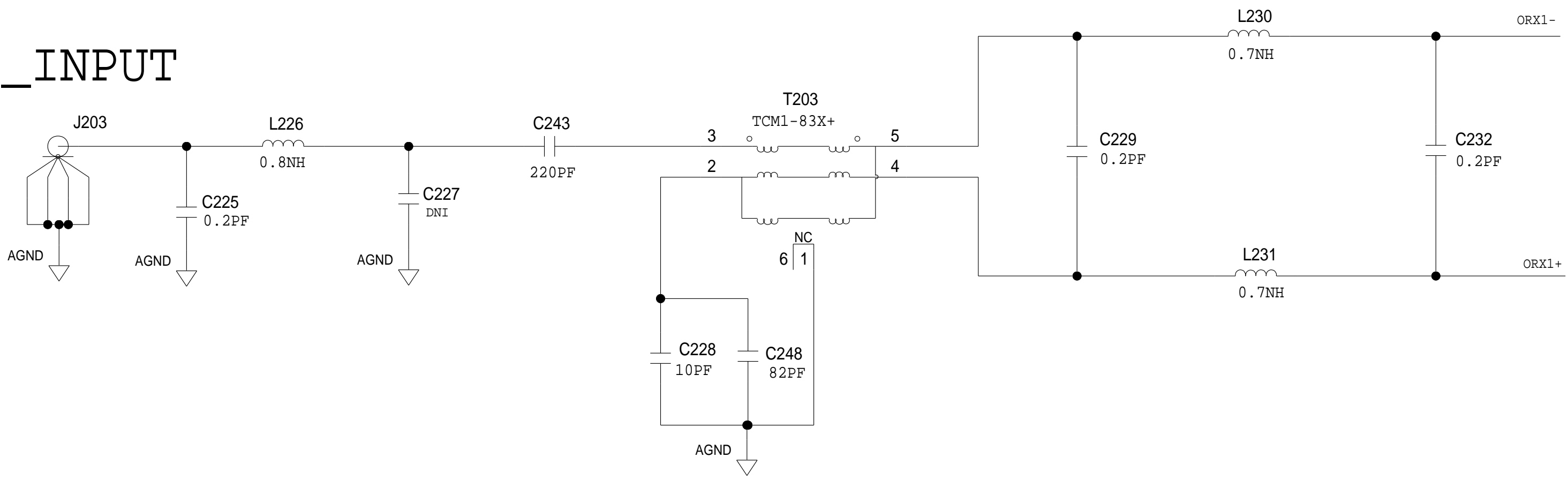
RF RX / ORX / SNIFFER INPUTS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

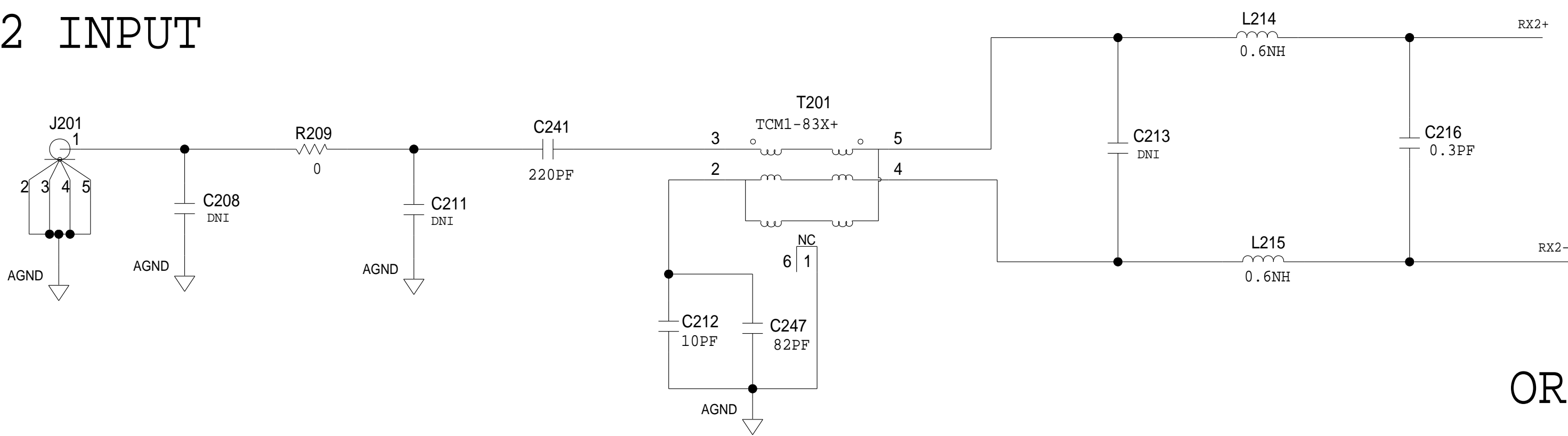
RX1 INPUT



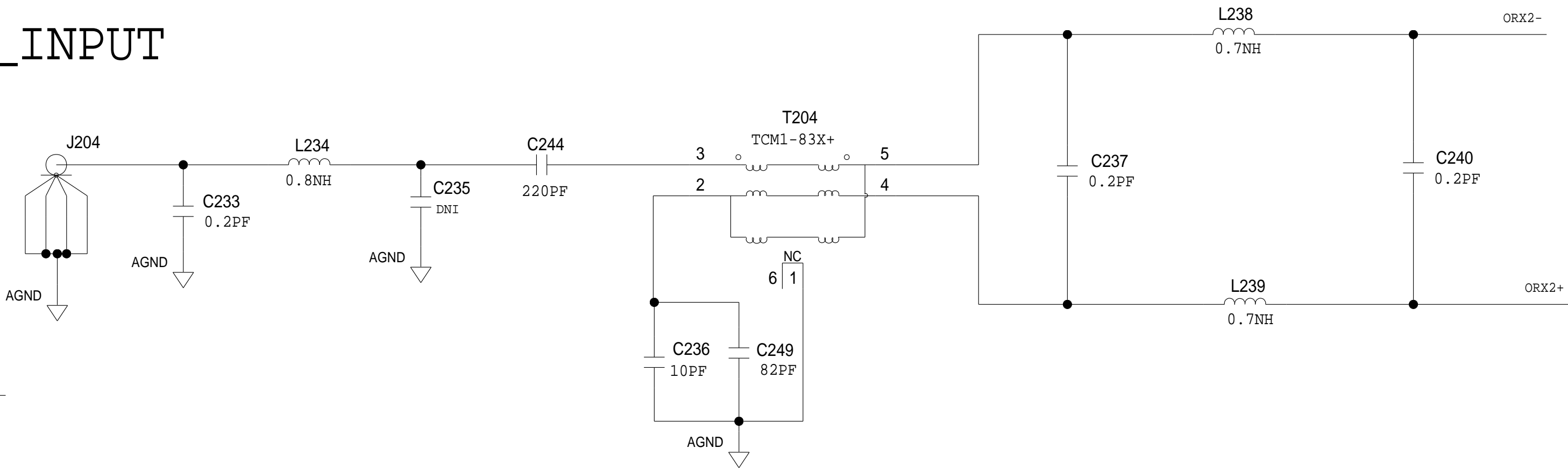
ORX1_INPUT



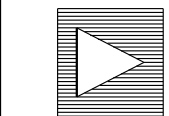
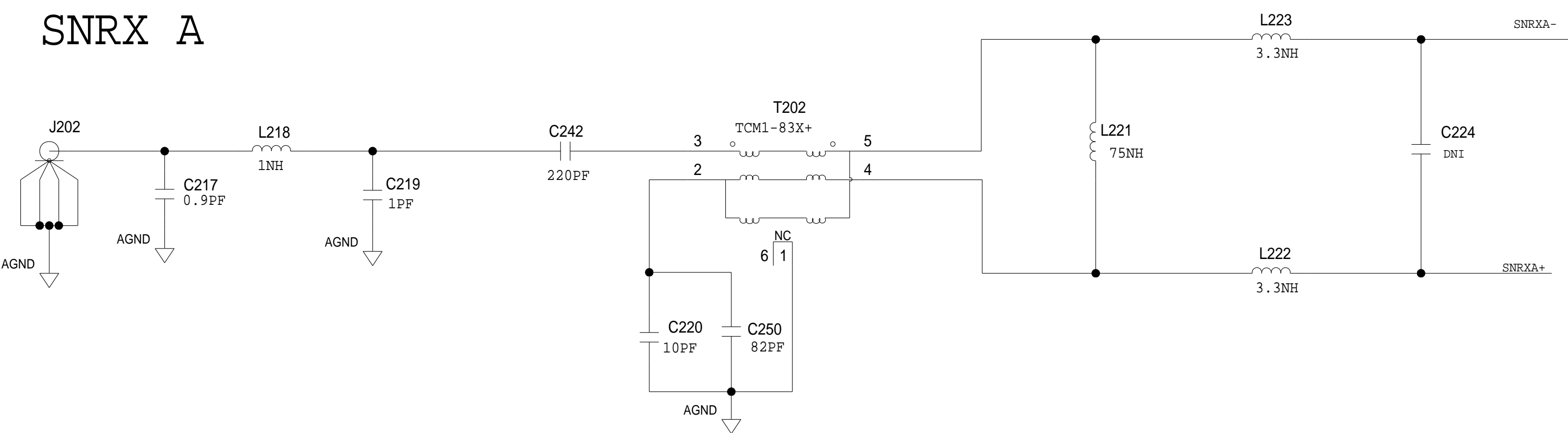
RX2 INPUT



ORX2_INPUT



SNRX A



ANALOG
DEVICES

THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC.
IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR
IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS,
OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): AD9371

DESIGN VIEW
<DESIGN_VIEW>
PTD ENGINEER
T KARPUS

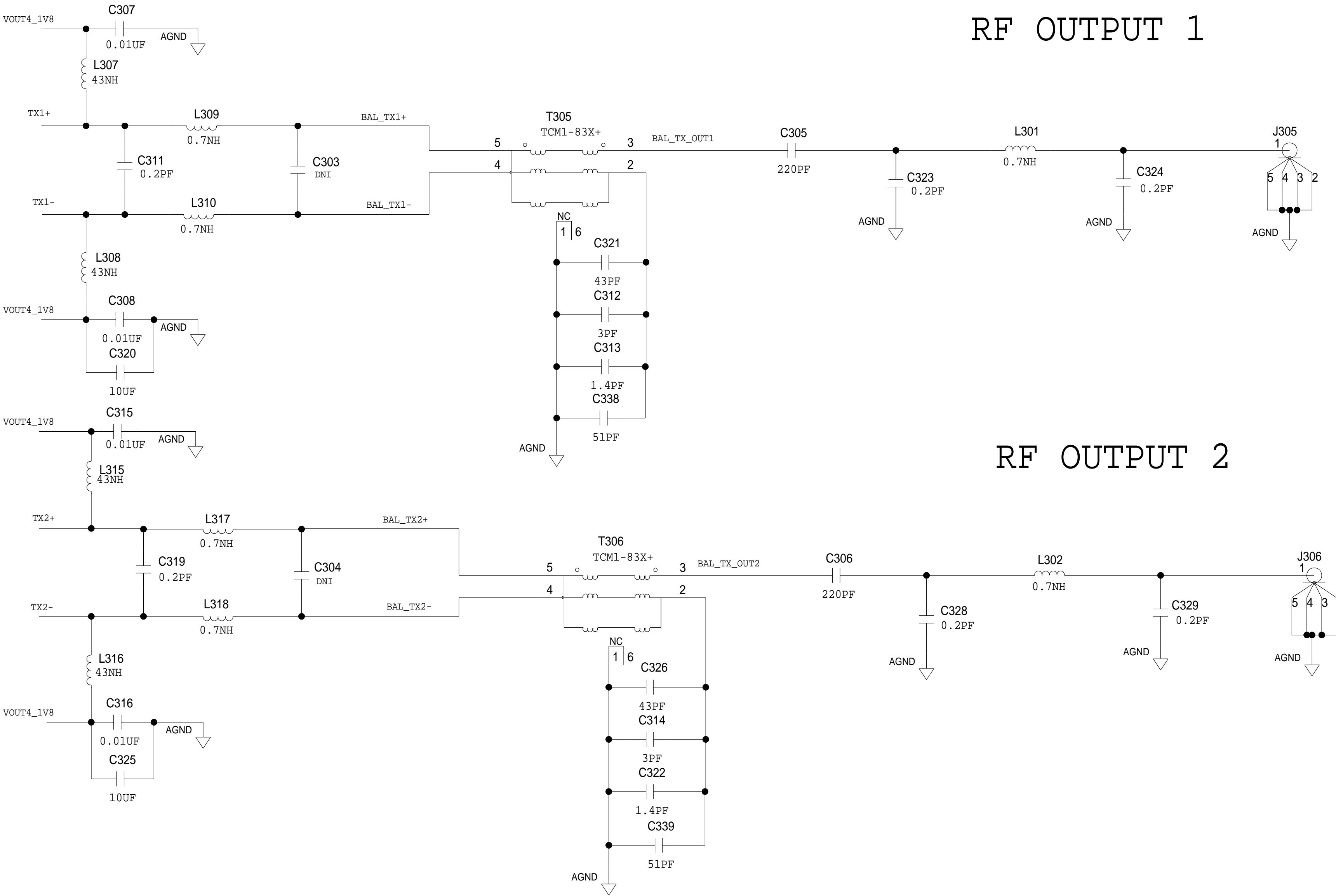
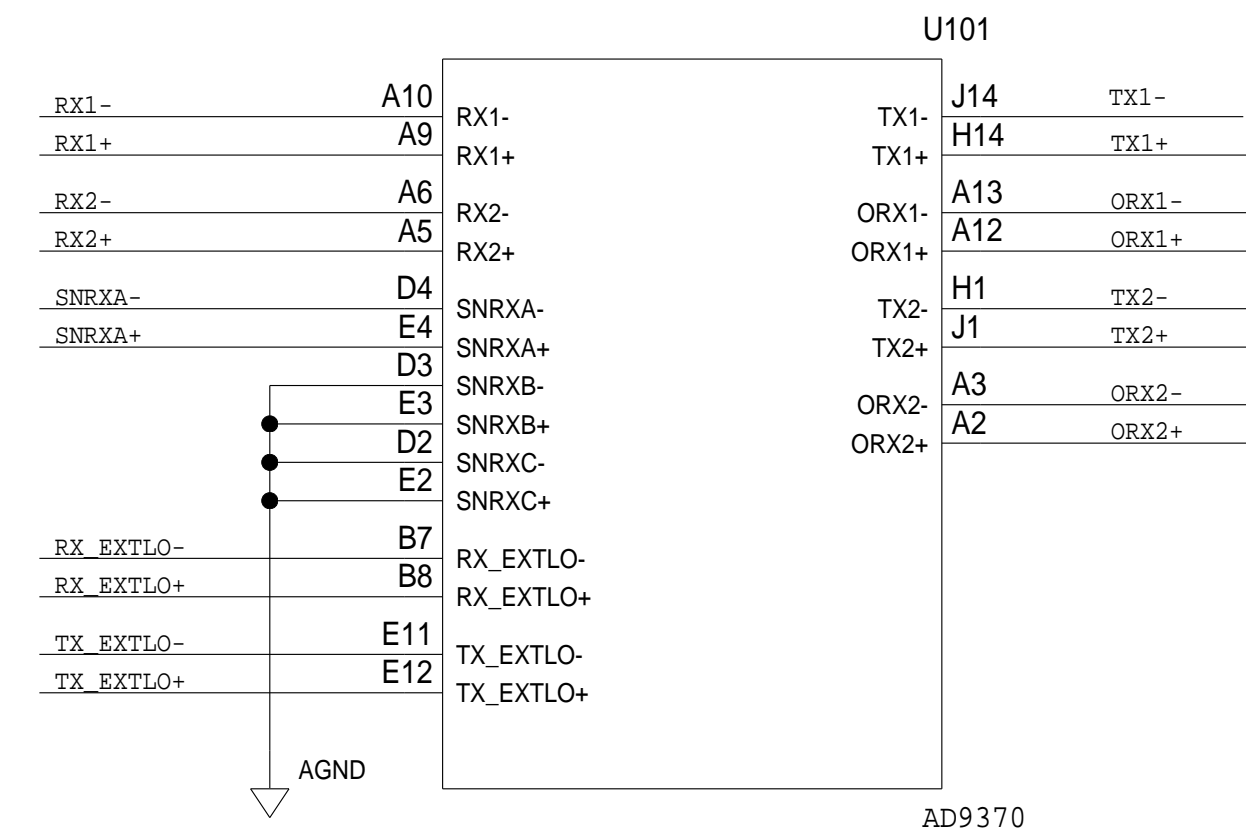
DRAWING NO.
02_042591

SIZE **D**
SCALE 1:1

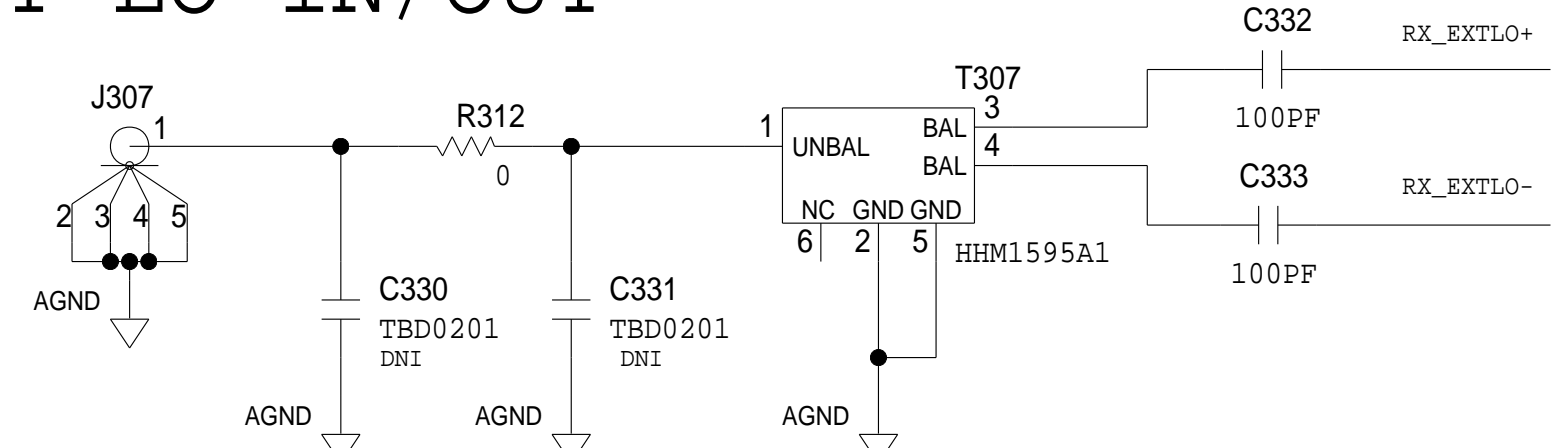
REV
B
SHEET 2 OF 8

RF TX OUT / EXT LO IN

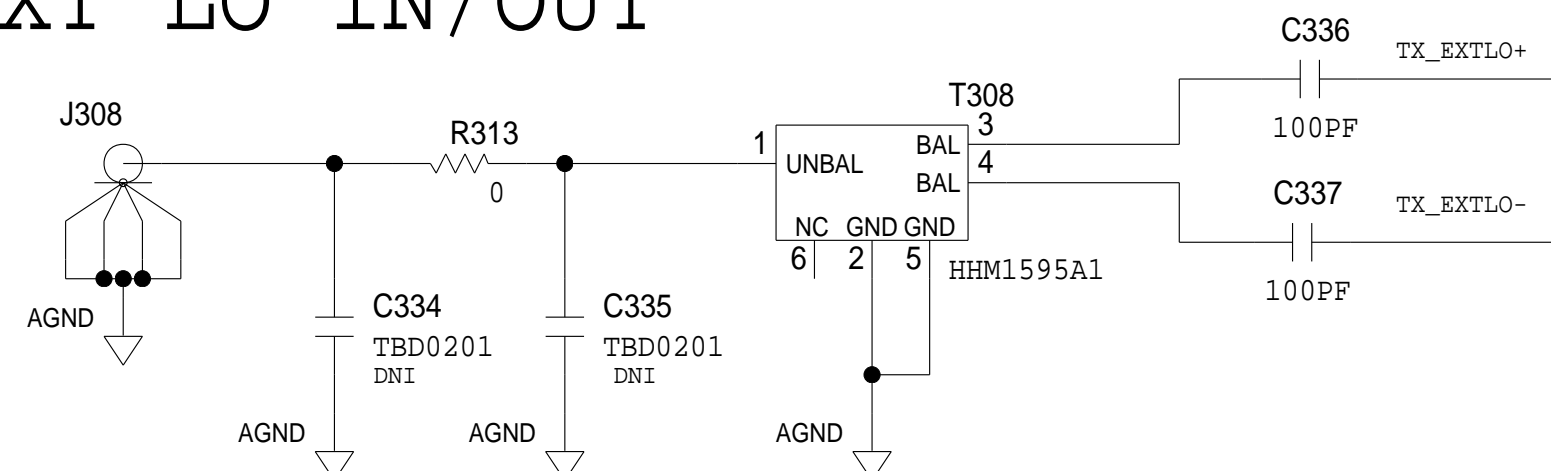
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



RX EXT LO IN/OUT

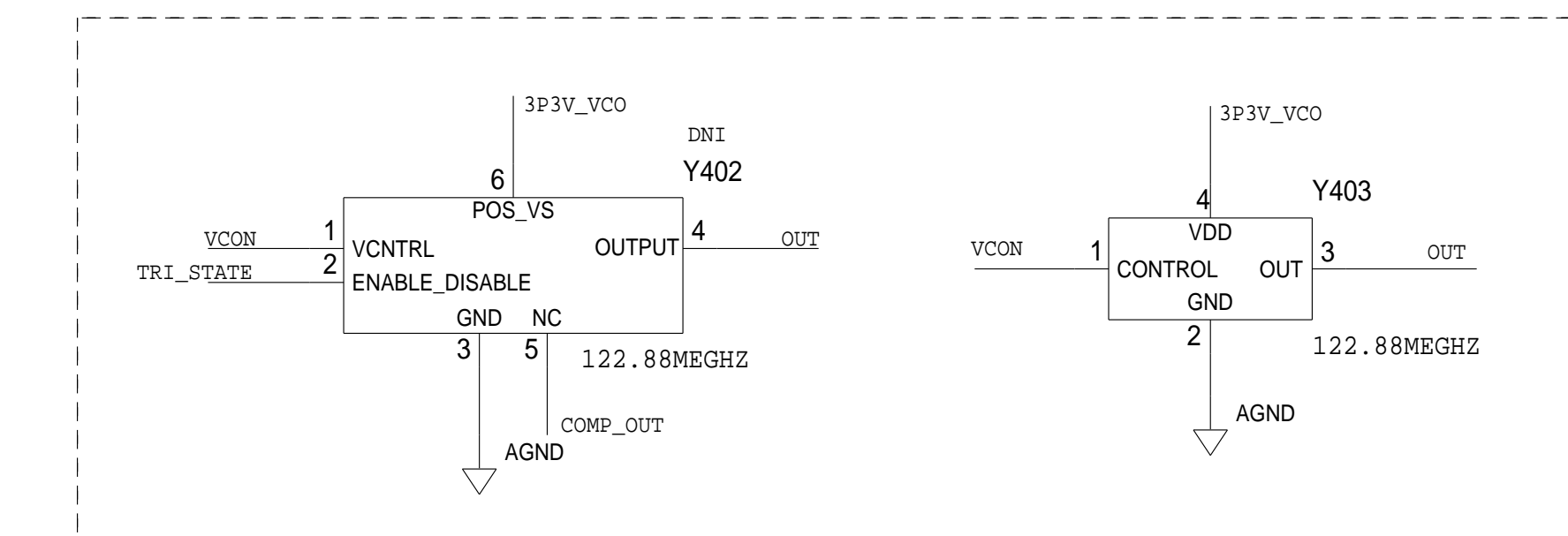
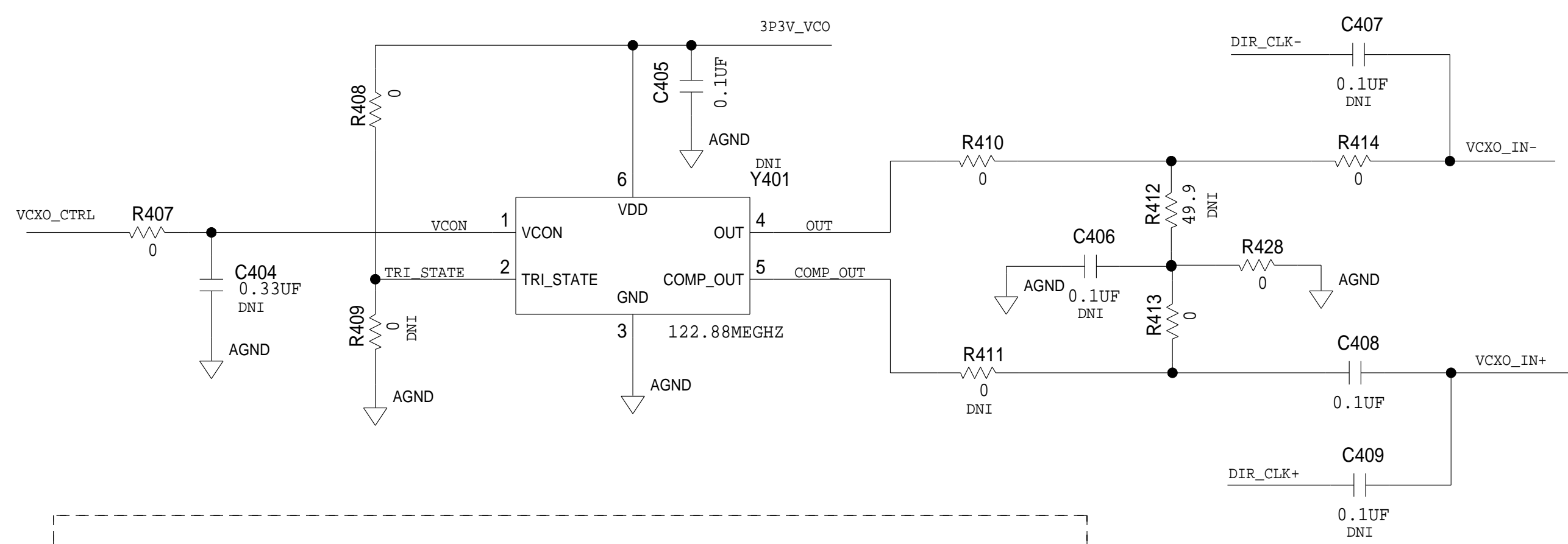
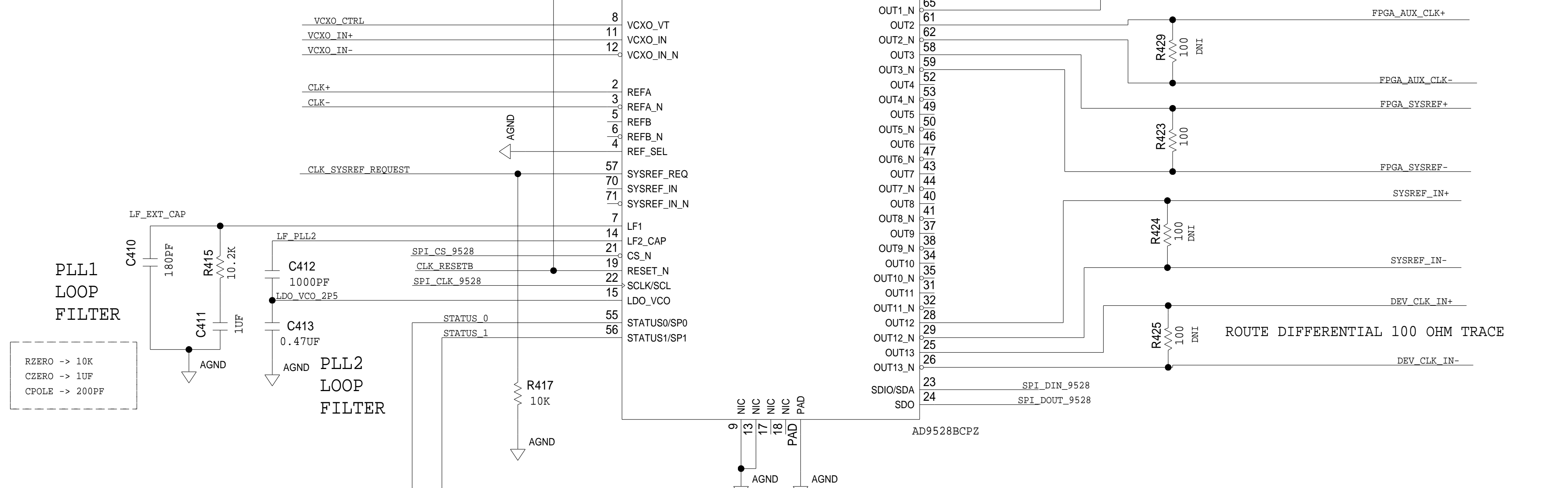
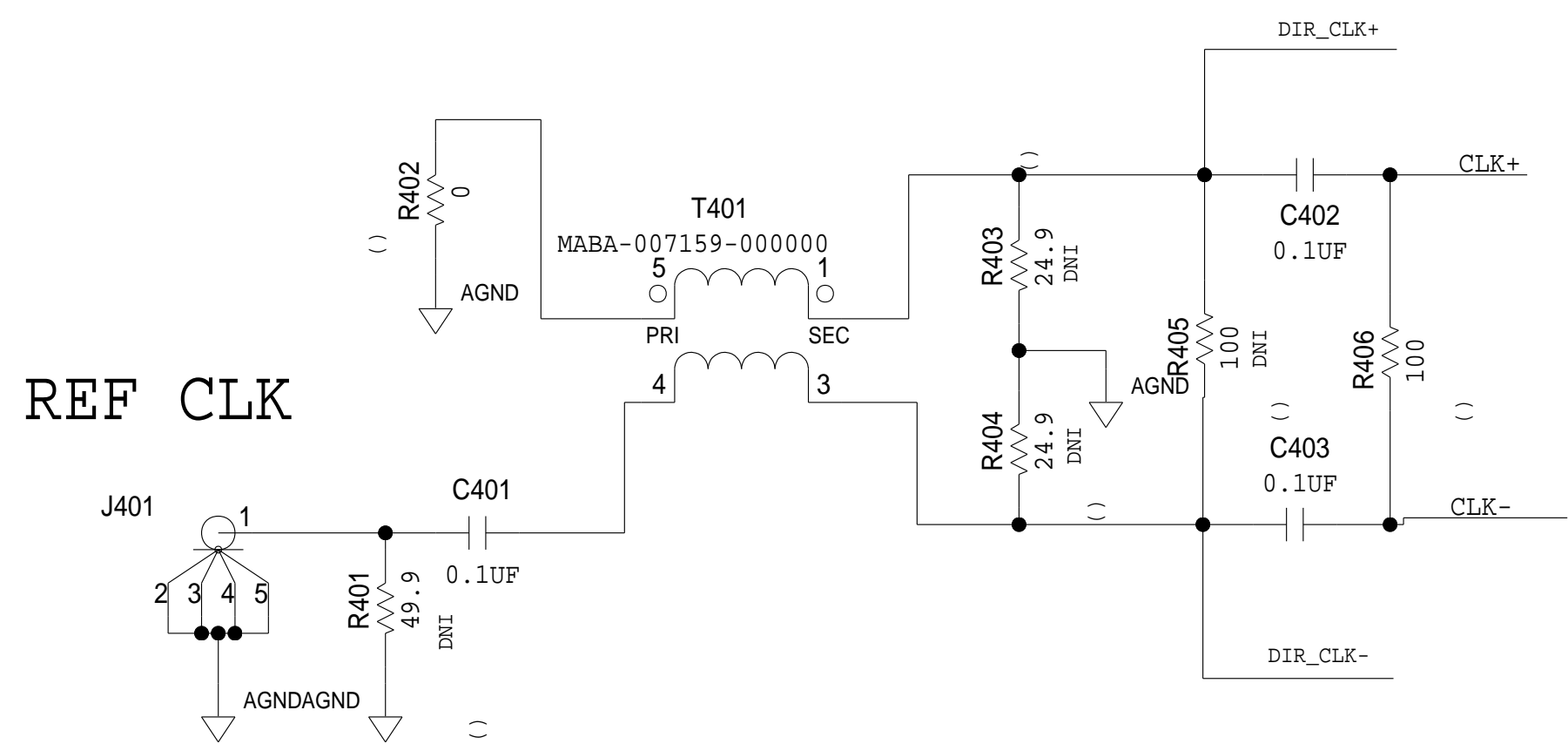


TX EXT LO IN/OUT

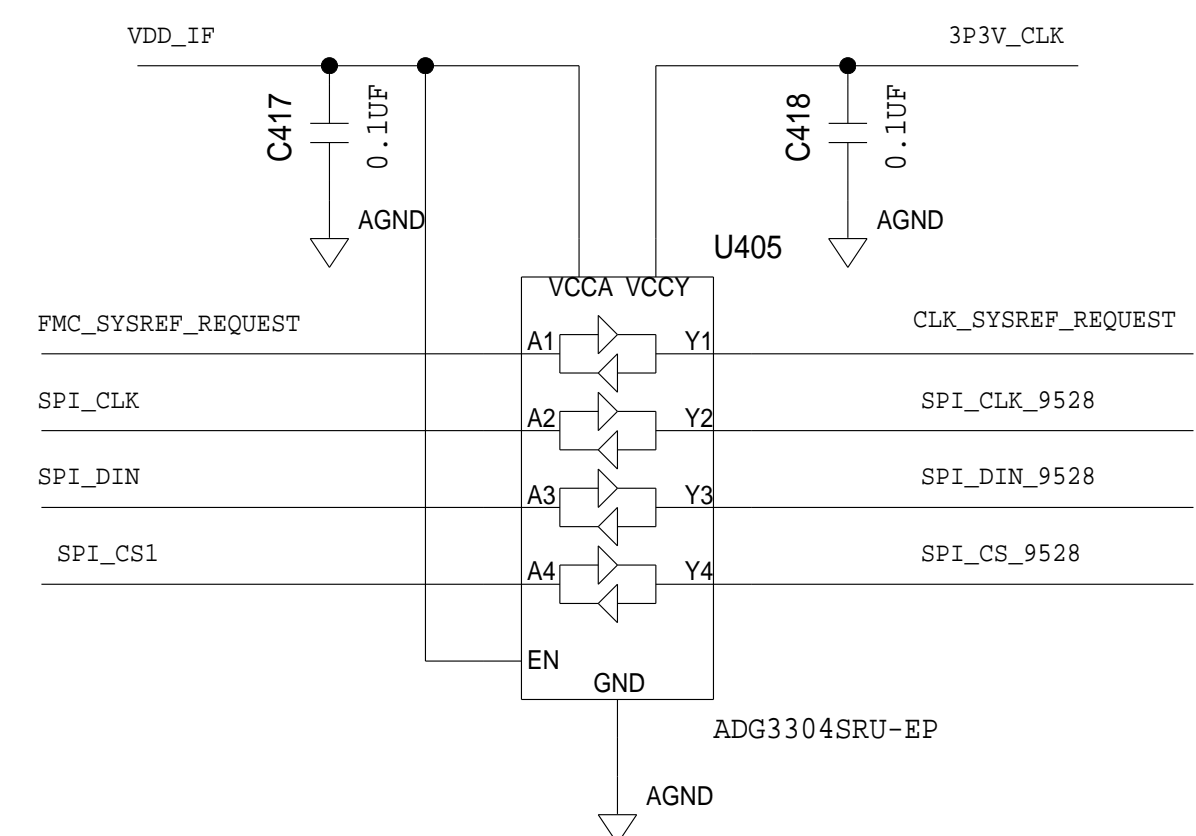
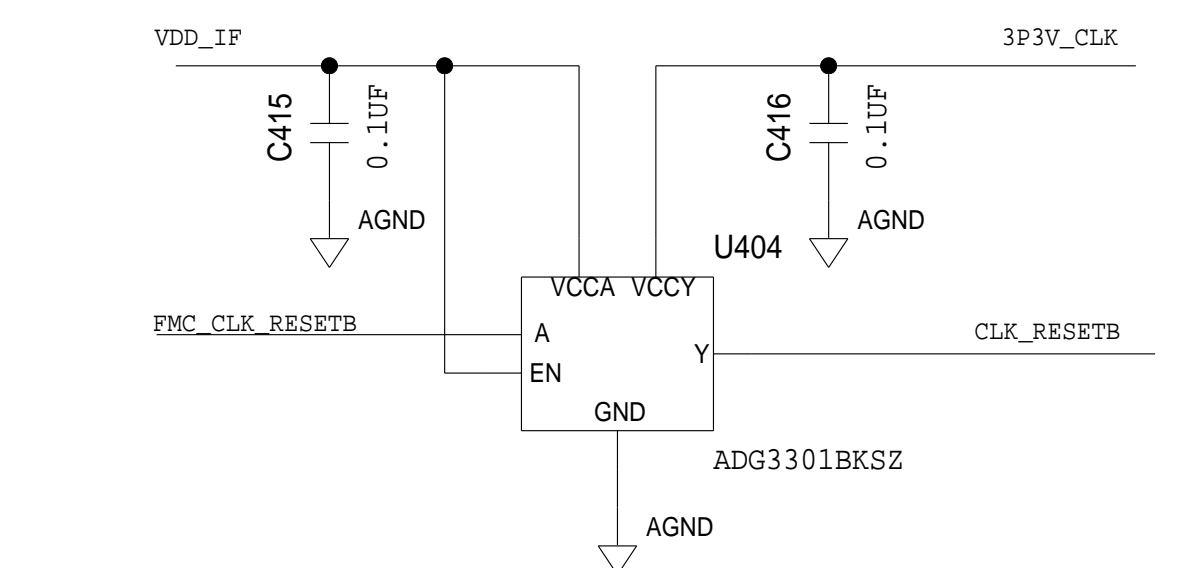
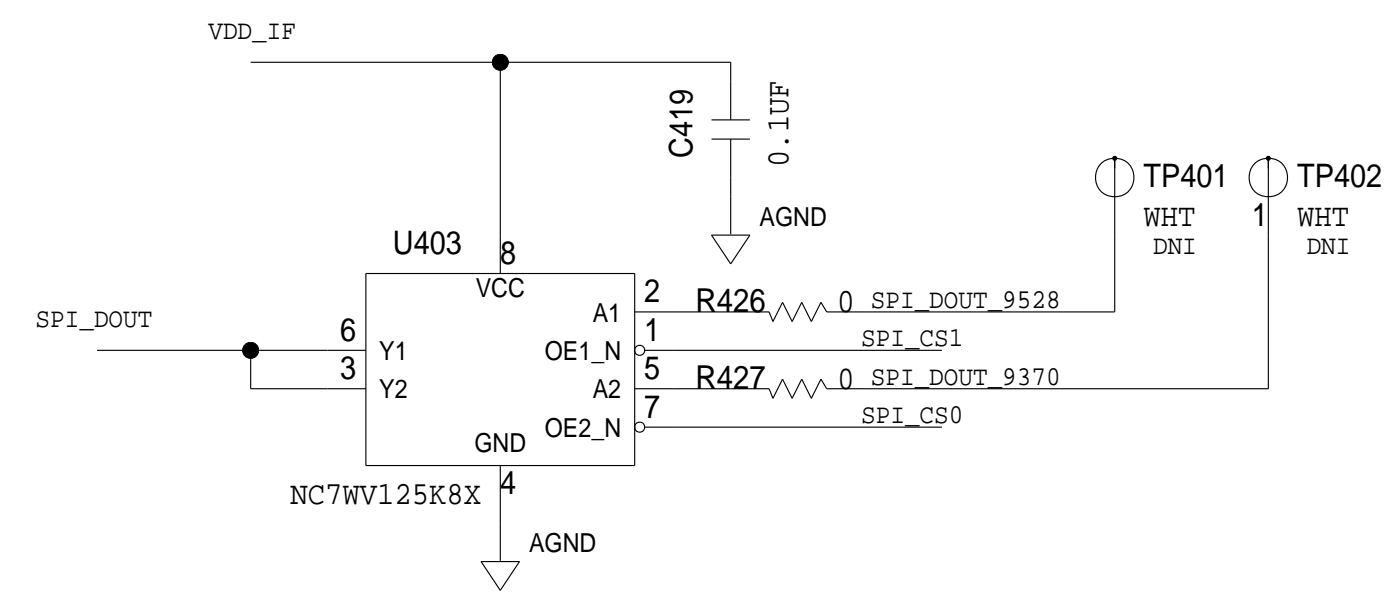
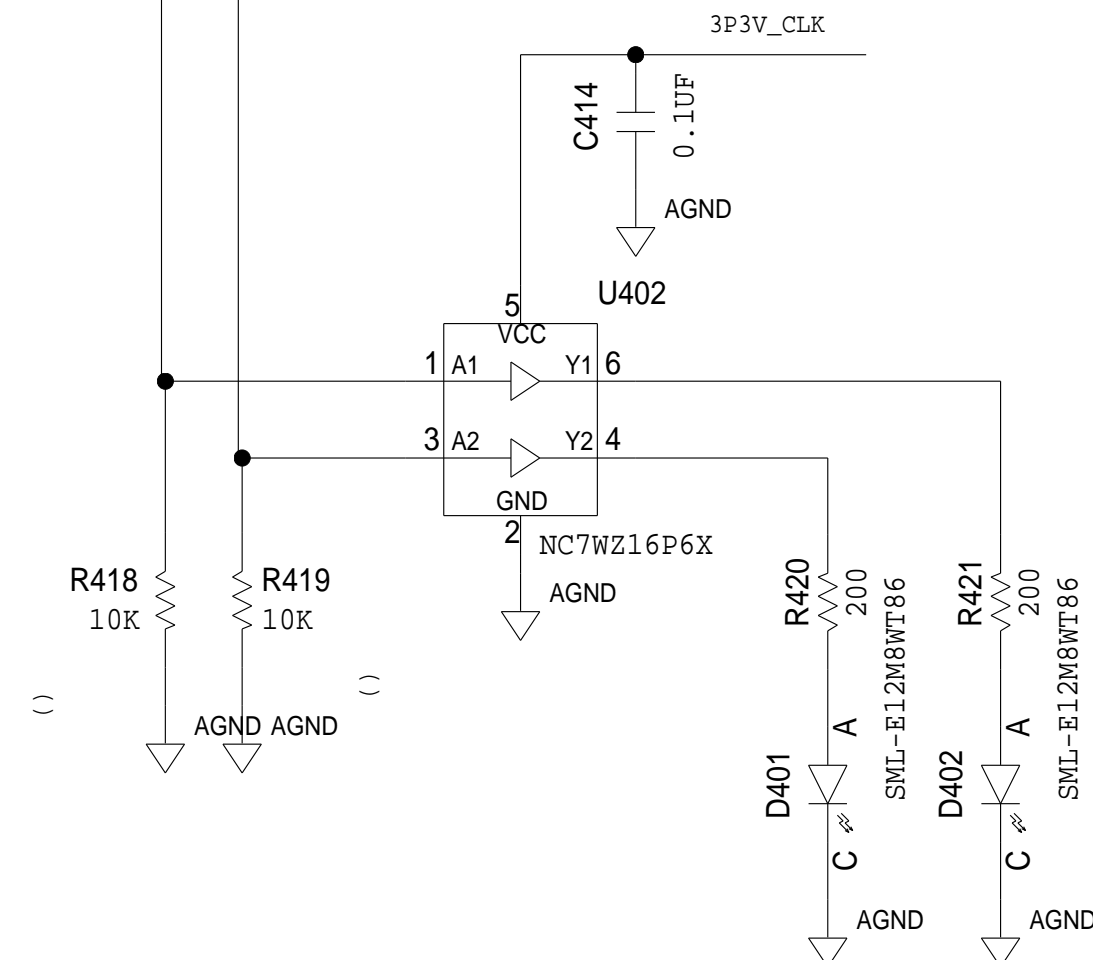
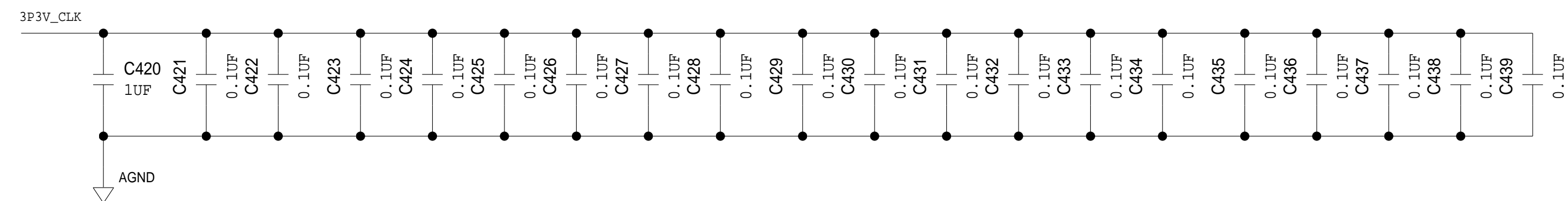


SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): AD9371			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_042591	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 3 OF 8


CLOCK GENERATION



FOOTPRINTS OVERLAP IN LAYOUT
FOR CRYSTAL PACKAGE OPTION



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

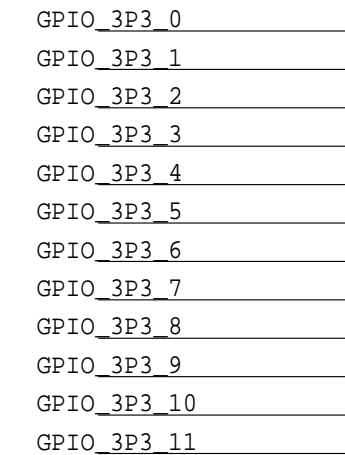
 ANALOG DEVICES	<h1 style="text-align: center;">SCHEMATIC</h1>			
	HW TYPE : Customer Evaluation Product(s) : AD9371			
<small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES, INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN CHANGING INFORMATION TO OTHERS. OR FOR ANY OTHER PURPOSES UNLESS, IN THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT AND/OR HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</small>	DESIGN VIEW <DESIGN_VIEW> PTD ENGINEER T KARPUS	DRAWING NO. 02_042591 SIZE D	SCALE 1:1	REV B SHEET 4 OF 8

1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

PLACE CAPACITORS
CLOSE TO THE FMC/FPGA

PLACE CAPACITORS
CLOSE TO THE FMC/FPGA



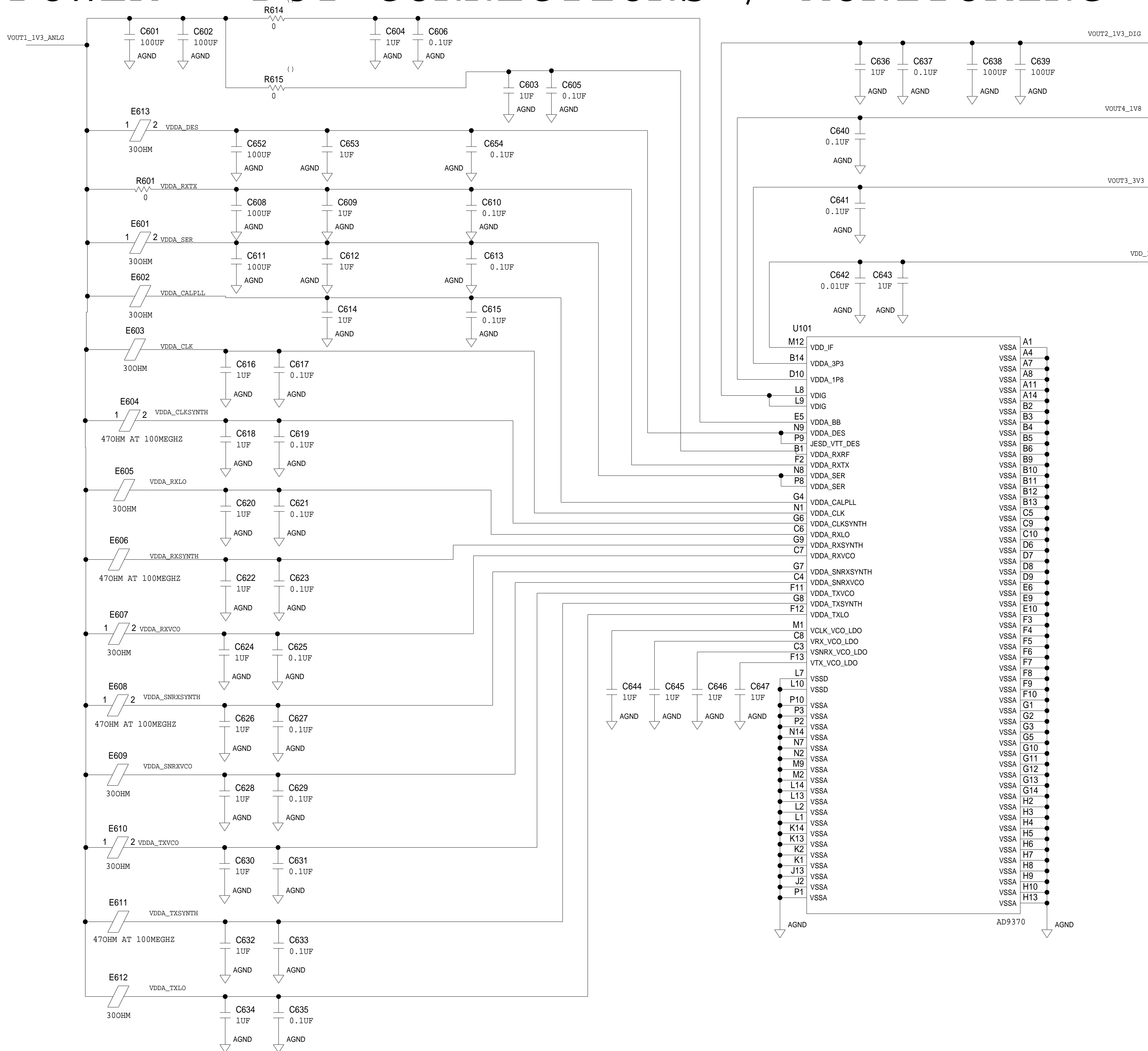
J-TAG INTERFACE

SIZE D	SCALE 1:1	SHEET 5 OF 8
------------------	--------------	--------------

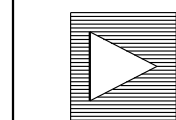
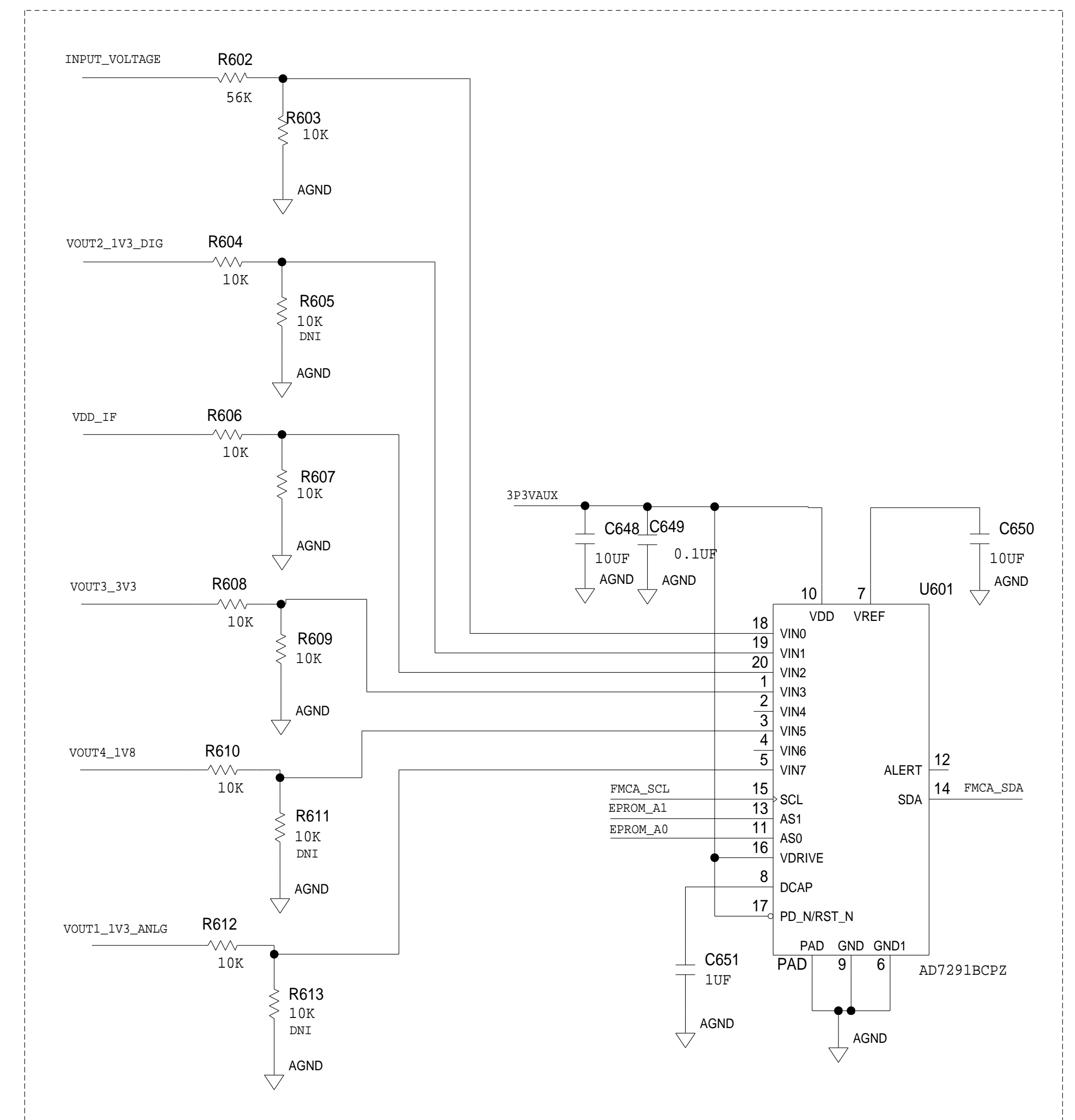
POWER - DUT CONNECTIONS / MONITORING

REVISIONS

REV	DESCRIPTION	DATE	APPROVED



POWER DOMAINS MONITORING ADC



ANALOG
DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation
Product(s) : AD9371

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
T KARPUS

DRAWING NO.
02_042591

SIZE
D

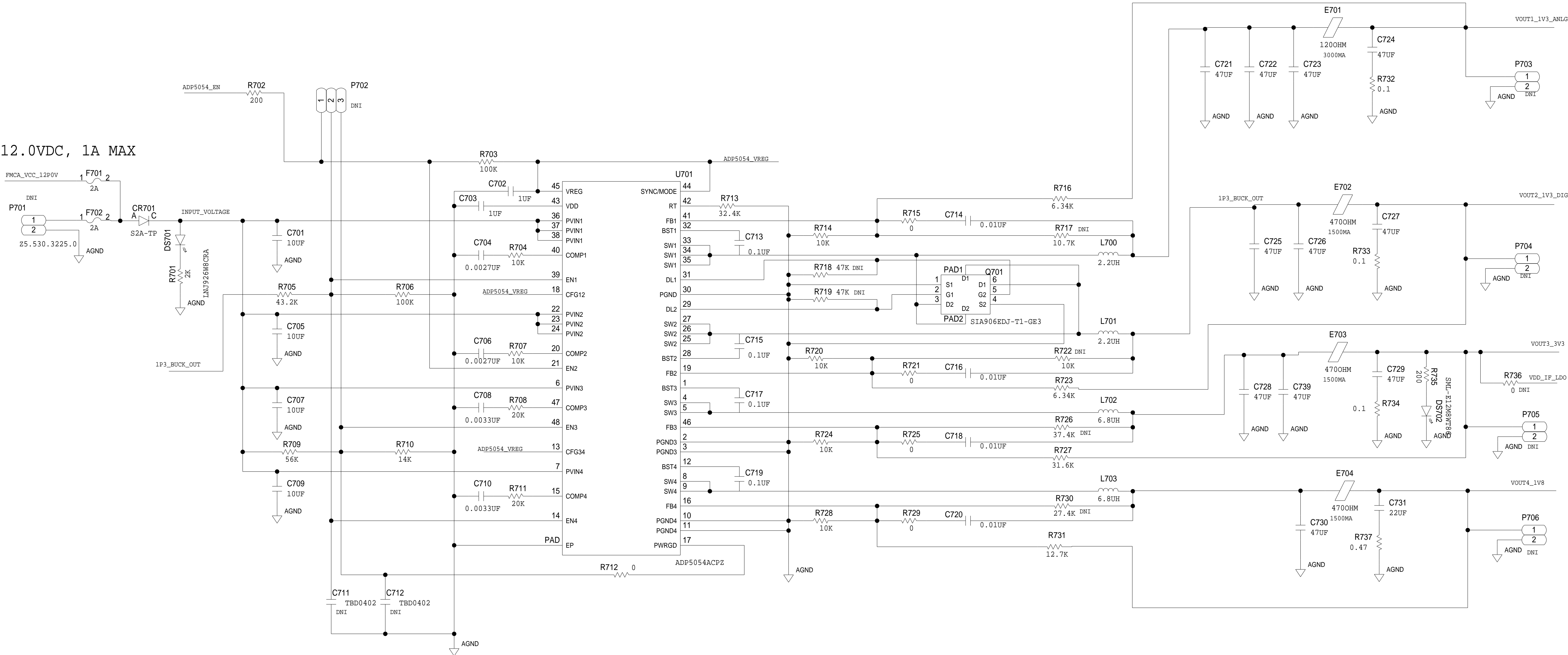
SCALE
1:1

REV
B

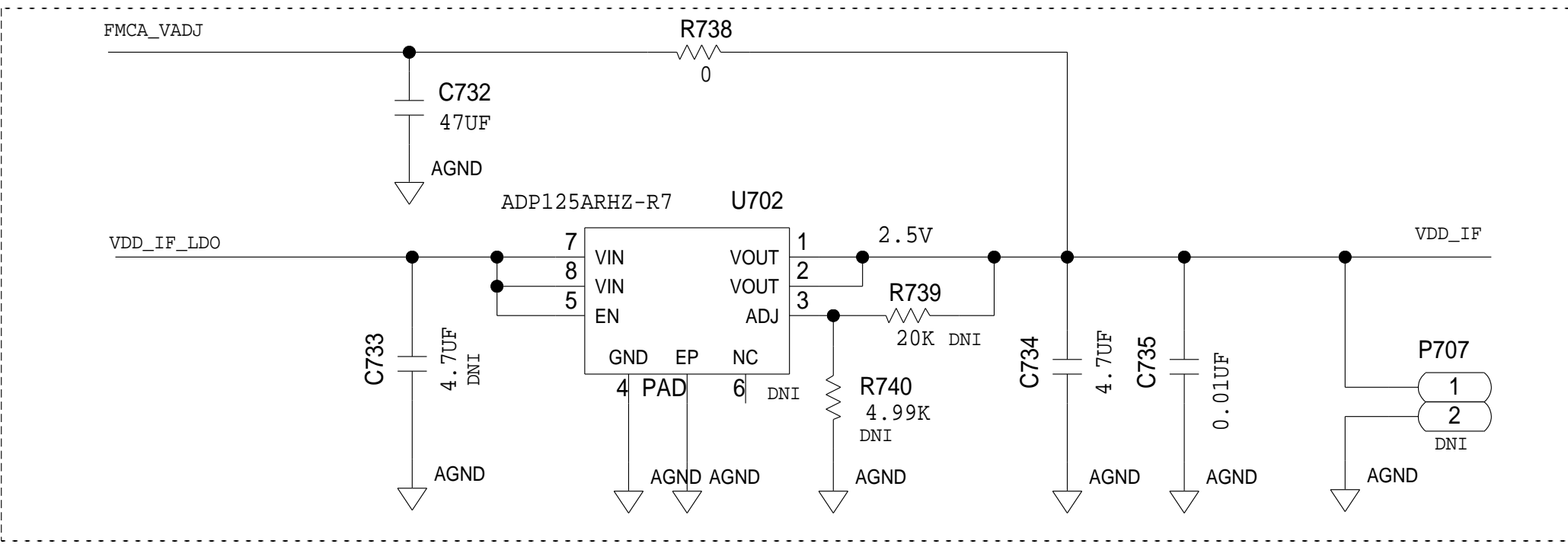
SHEET 6 OF 8

POWER SUPPLY

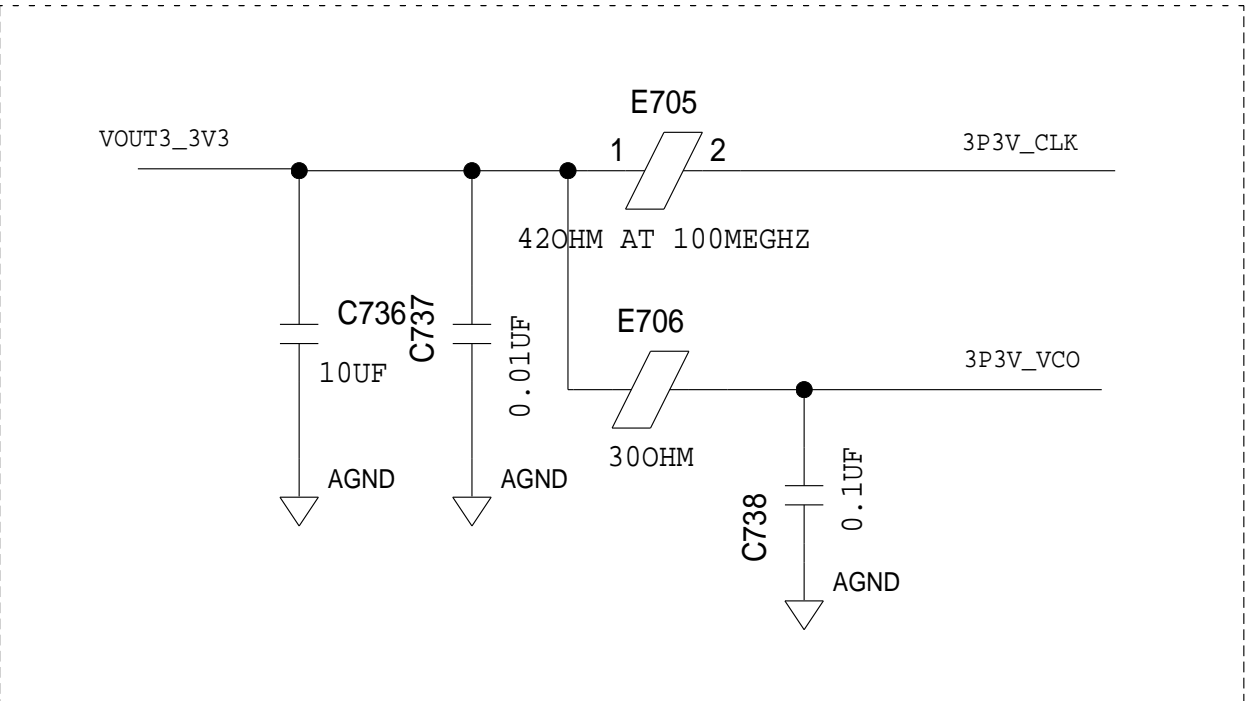
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



INTERFACE SUPPLY



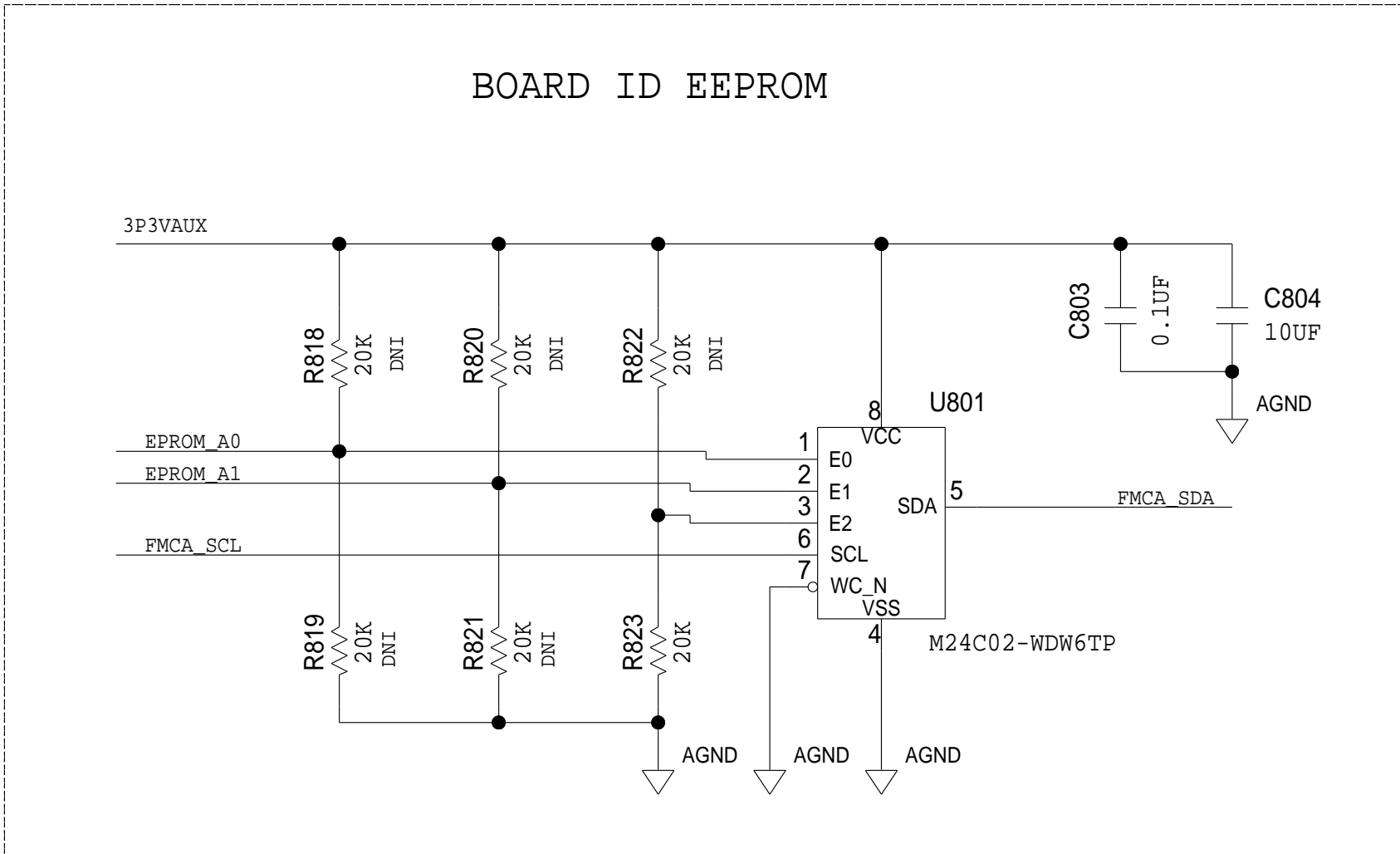
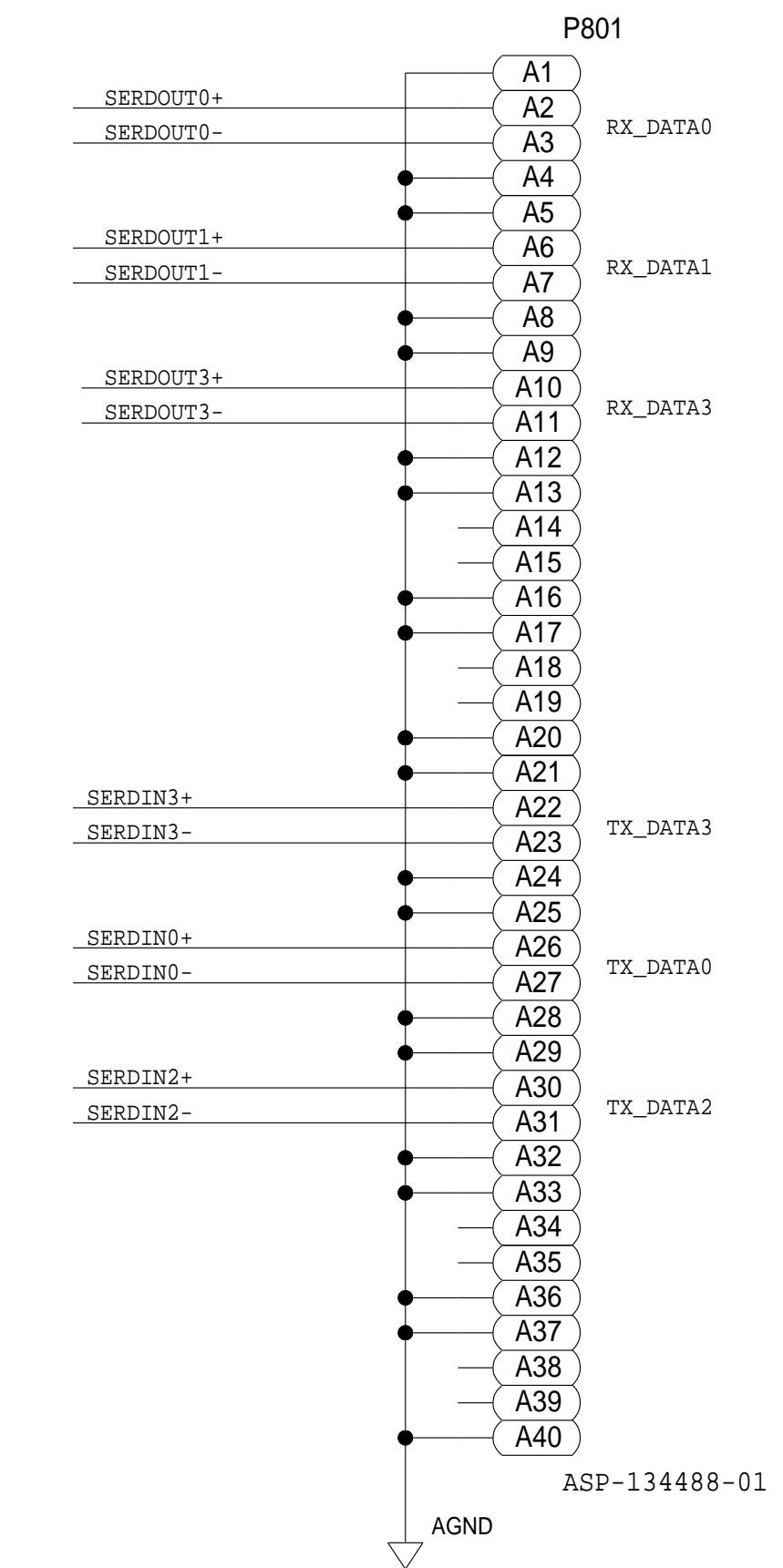
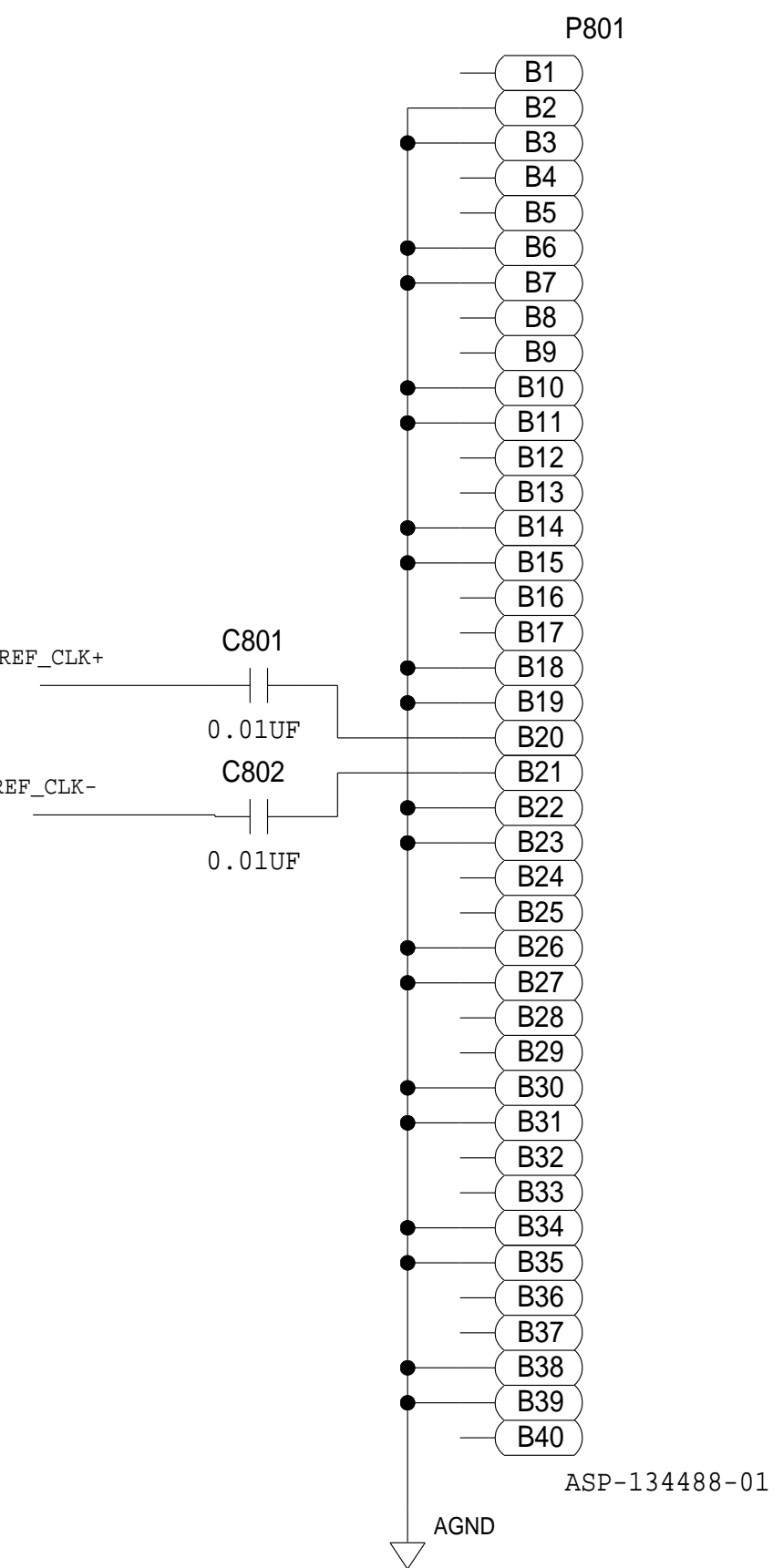
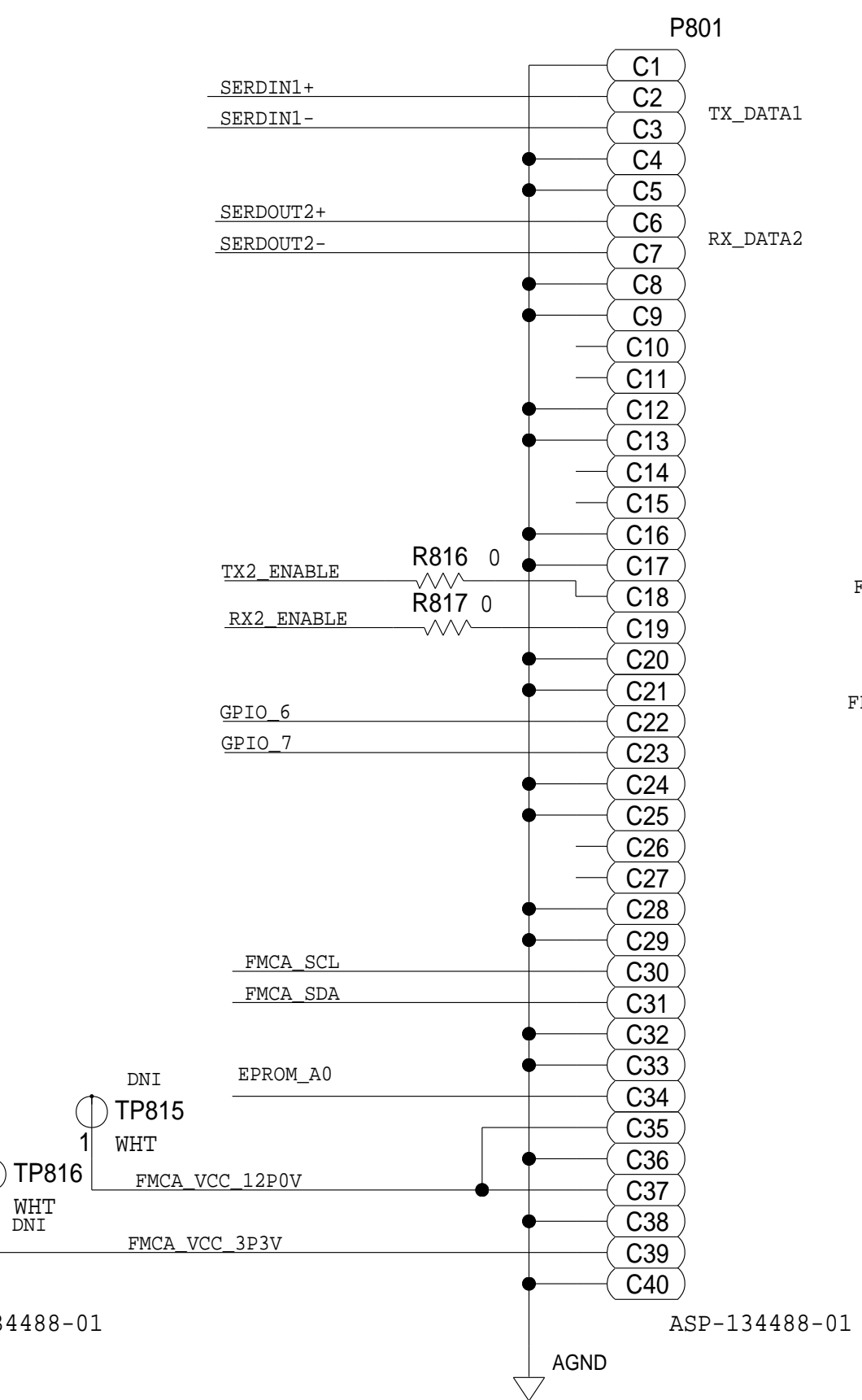
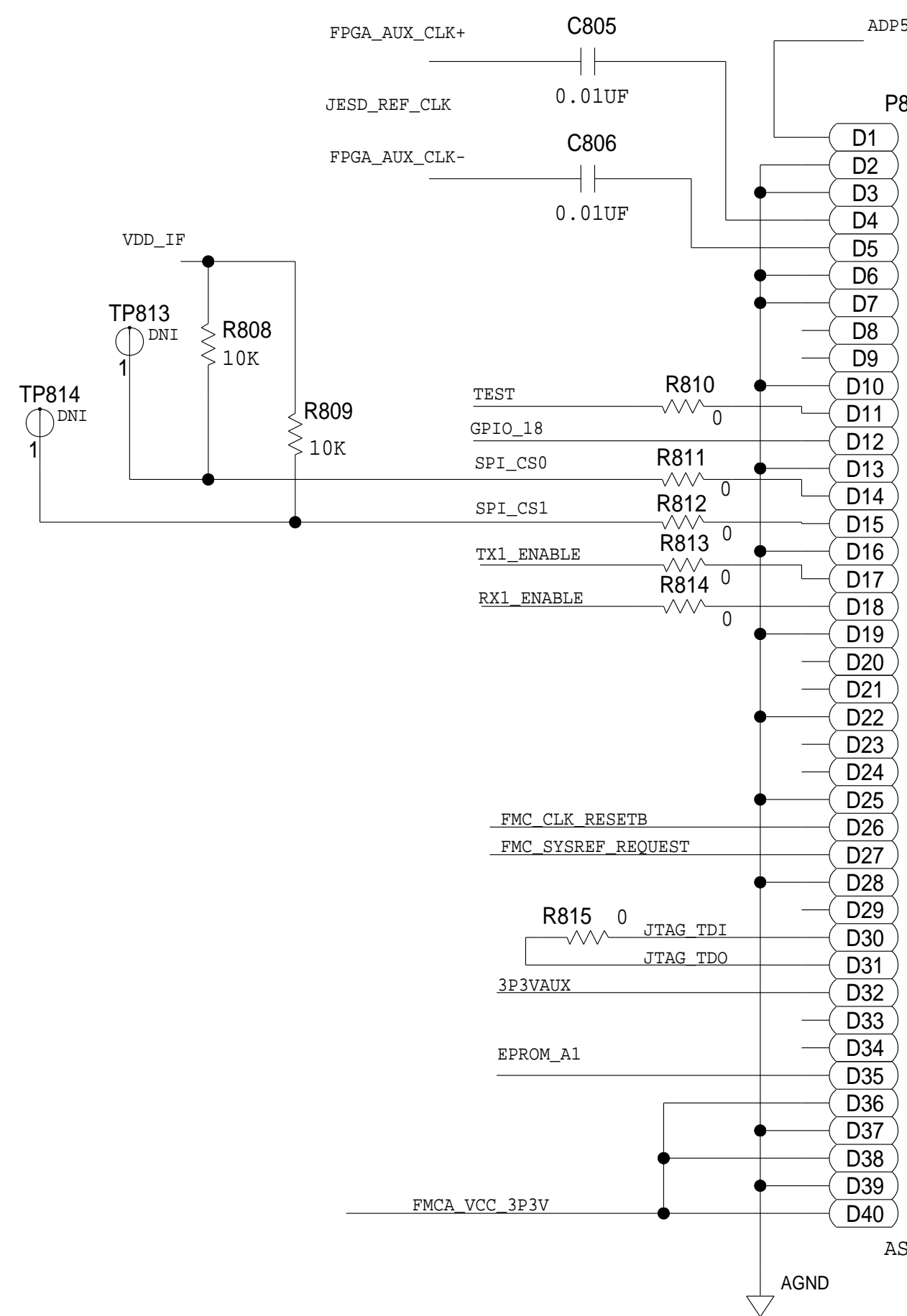
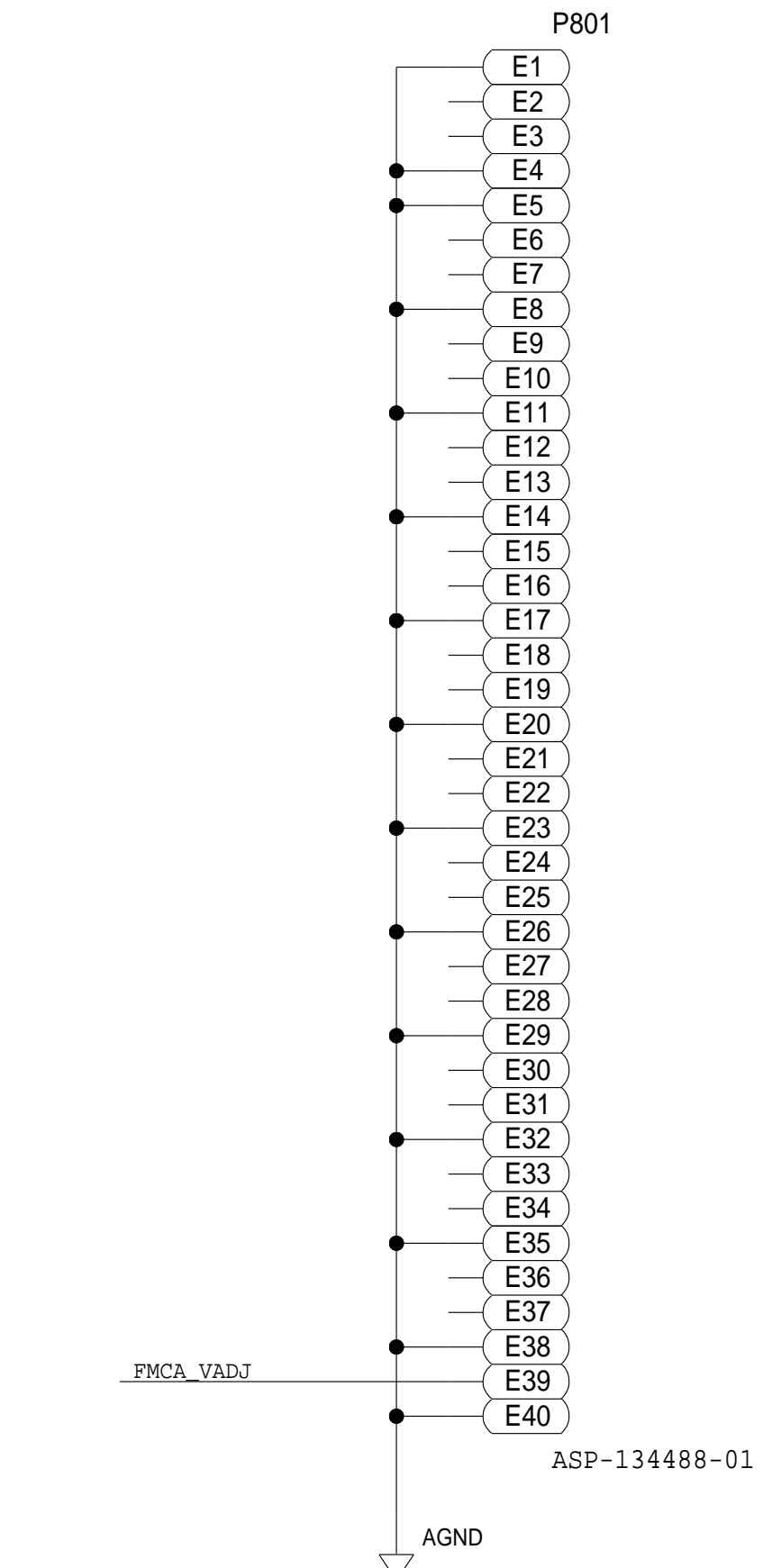
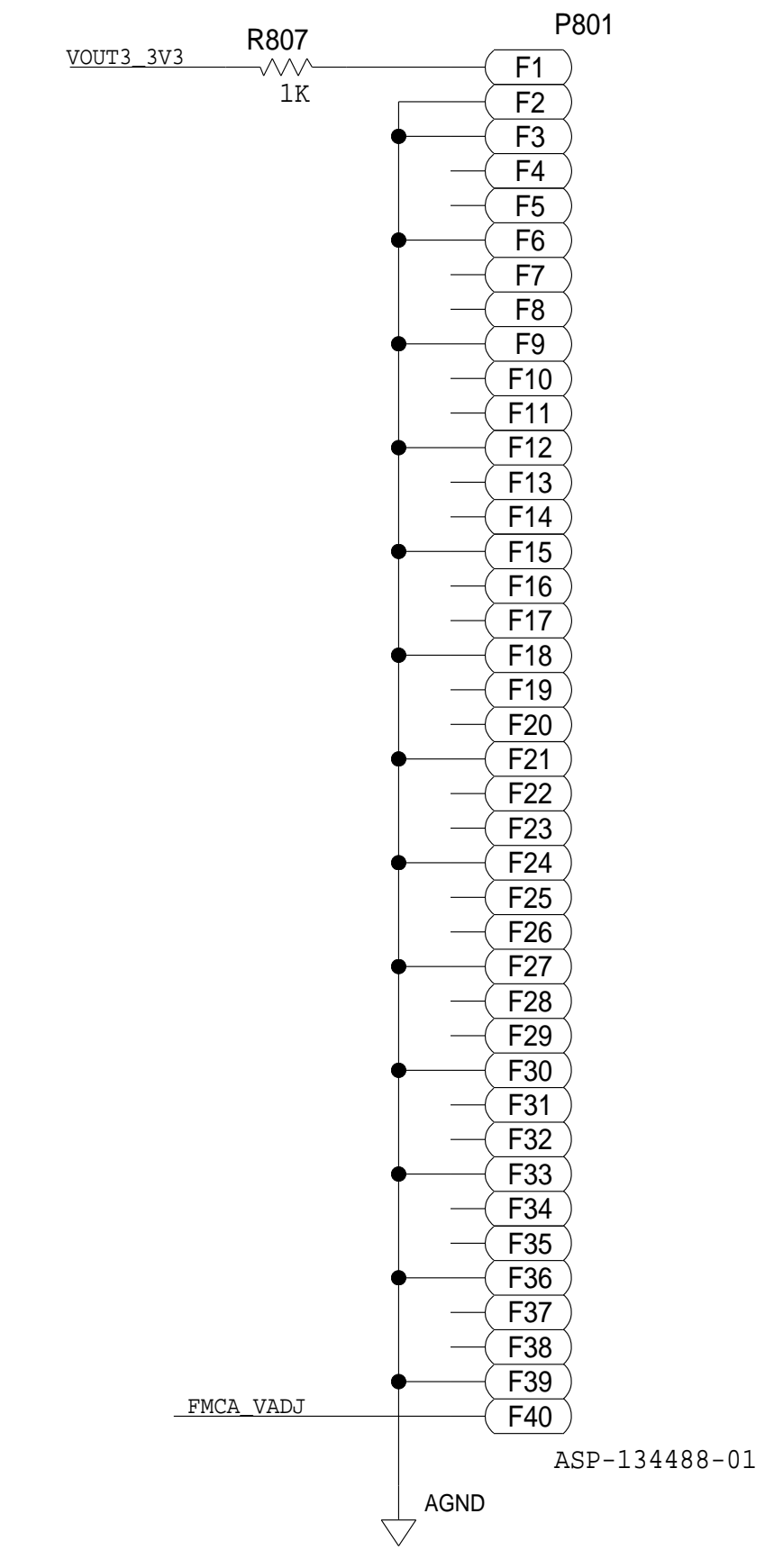
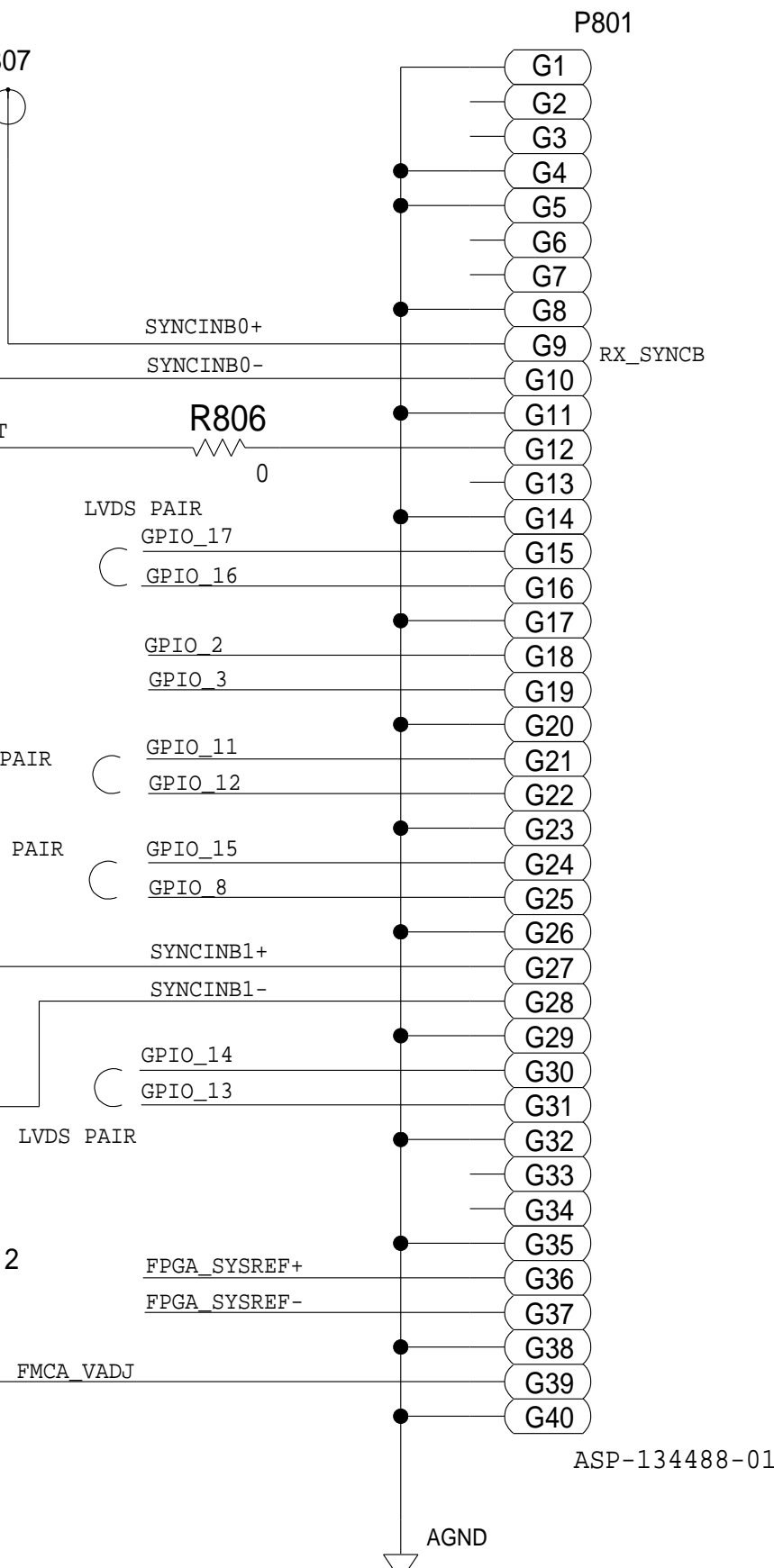
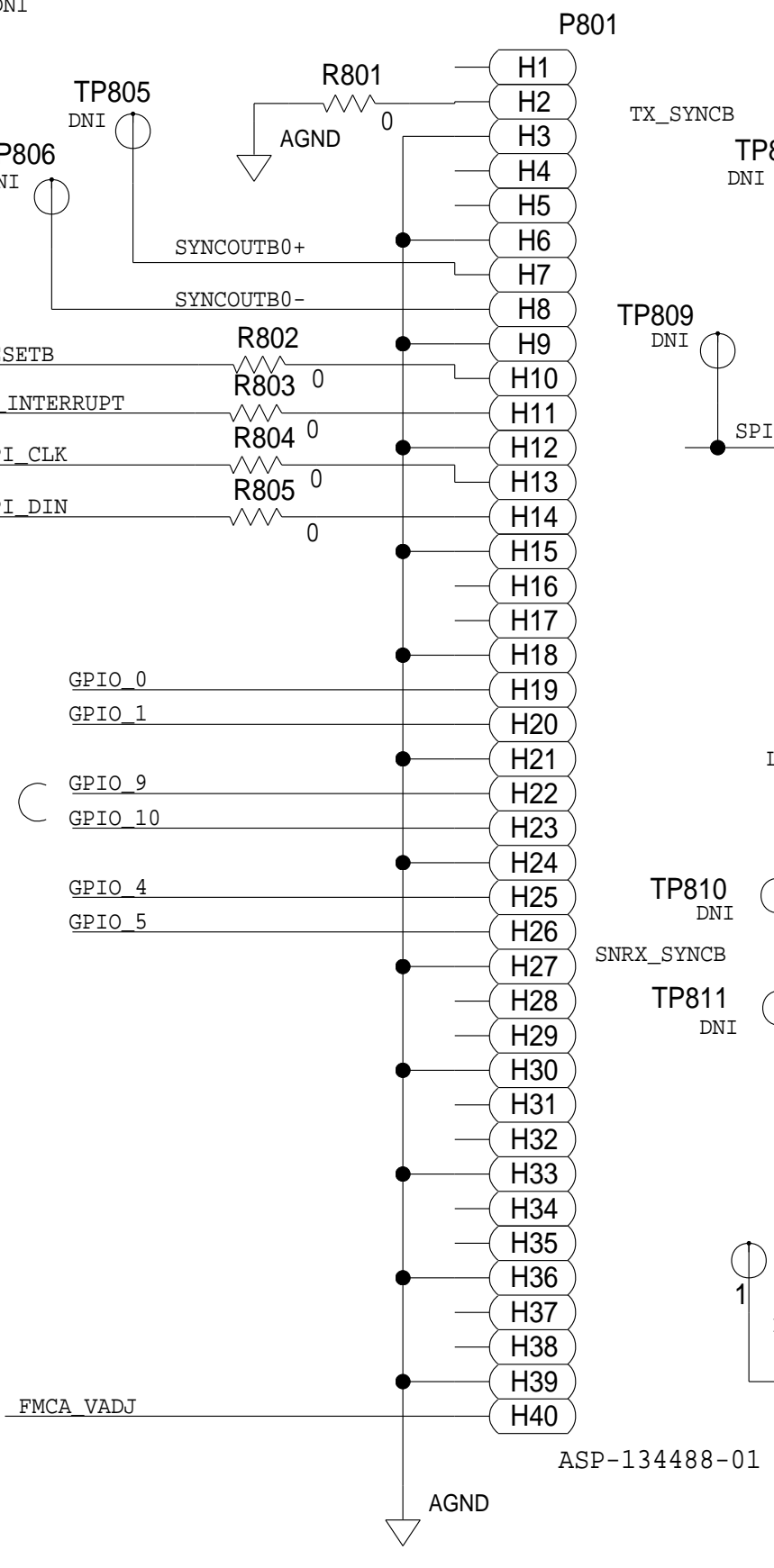
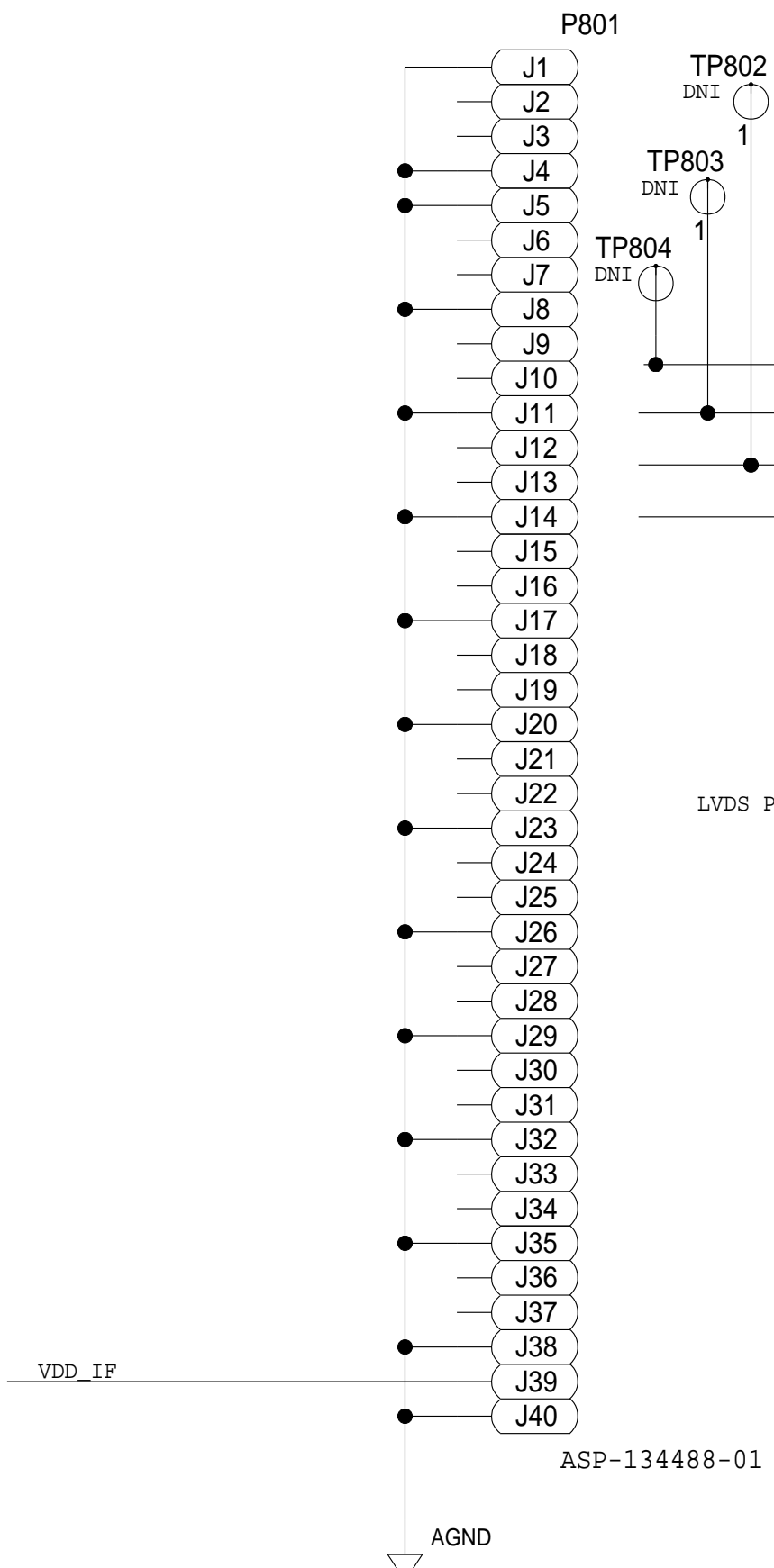
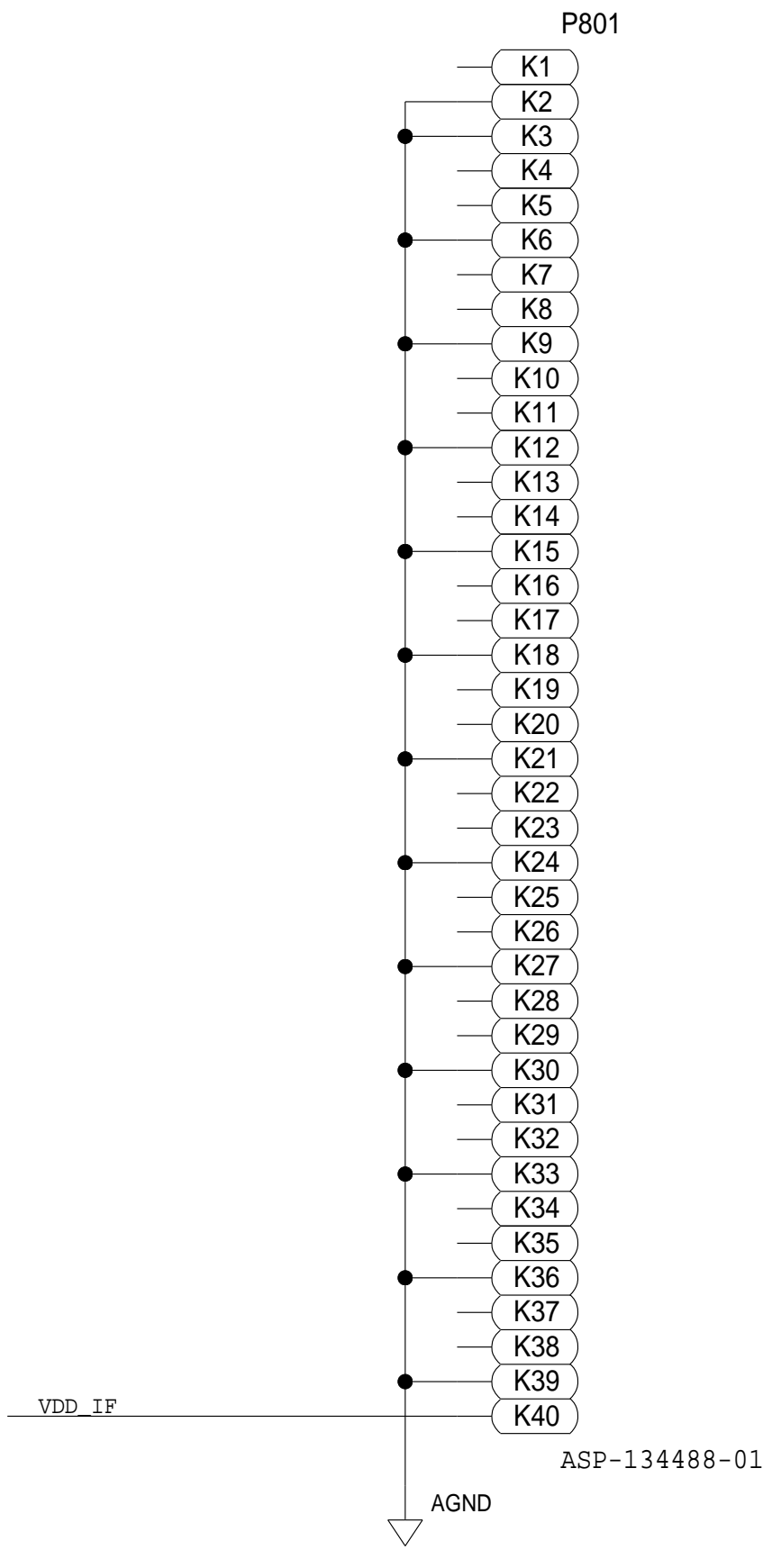
CLOCK SUPPLY



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): AD9371			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_042591	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 7 OF 8

FMC – FPGA CONNECTIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): AD9371			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_042591	REV B	
PTD ENGINEER T KARPUS	SIZE D	SCALE 1:1	SHEET 8 OF 8